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For: **IMAGE SENSING STRUCTURE**

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Sir:

Transmitted herewith is a certified copy of the priority European Application No.03251149.5.

Respectfully submitted,

Michael W. Taylor

MICHAEL W. TAYLOR
Reg. No. 43,182
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
Telephone: 407/841-2330
Fax: 407/841-2343
Attorney for Applicant

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Anmelder/Applicant(s)/Demandeur(s):

STMicroelectronics Limited
Planar House,
Parkway,
Globe Park
Marlow,
Buckinghamshire SL7 1YL
GRANDE BRETAGNE

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Image sensing structure

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Image Sensing Structure

The present invention relates to an image sensing structure, and in particular but not exclusively to an image sensing structure comprising a photodiode that provides highly accurate matching between pixels.

Due to tolerances in the manufacturing process of photodiodes used in solid state imaging devices, there is usually a mismatch in sensitivity between pixels. In the case of a camera that takes pictures to be viewed by humans, the tolerances can be relatively low while creating an image of acceptable accuracy. A mismatch of around five percent is acceptable. However, for other applications such as cameras used for machine vision or optical mice, the allowable mismatch is much less, typically around one percent.

The classical way of ameliorating such a mismatch is to remove it at a system level using calibration and

compensation techniques. However, calibration requires special setup and also storage of the compensation coefficients, while compensation requires real-time processing, costing silicon and consuming power. Hence, both these techniques are complex to perform and are expensive.

As the areas of technology requiring an ameliorated mismatch are areas which are commercially expanding, there is a need for a photodiode structure that provides improved matching between pixels.

According to the present invention there is provided a photodiode as claimed in the attached claims.

The present invention shall now be described, by way of example only, with reference to the accompanying drawings, in which:

Fig. 1 shows a first prior art image sensing structure;

Fig. 2 shows a second prior art image sensing structure;

Fig. 3 shows an image sensing structure in accordance with a first embodiment of the present invention;

Fig. 4 shows an image sensing structure in accordance with a second embodiment of the present invention; and

Fig. 5 shows an image sensing structure in accordance with a third embodiment of the present invention.

In transistor fabrication, multiple transistors of similar conductivity types are commonly located in a single well. In normal use, the well is reverse biased with respect to the transistor and the substrate and there is virtually no current flowing into or out of the well and transistor. The transistors therefore do not interact, and so the electrical properties of the well are usually ignored.

However, the situation with photodetectors is very different. Incident light creates a current that flows into and/or out of the well, and the well's capacitance often determines the photodetector's sensitivity. Thus, the electrical properties of the well are very important to the operation of the detector.

In a CMOS image sensing structure, the voltage out is governed by the equation:

Voltage out = (number of photons x quantum efficiency x time x electronic charge) / capacitance of the sense node).

As the light collection (number of photons), conversion (quantum efficiency) and collection

process is largely the same for all pixels, the variation in the capacitance of the sense node is the main cause of variations in sensitivity.

These variations are due to manufacturing tolerances, and are fixed for a particular sensor, giving the name "Fixed Pattern Noise" (FPN). As the variation is fixed and not random, it is more accurately called Photo Response Non-Uniformity (PRNU).

Fig. 1 shows a common form of CMOS image sensing structure. An epitaxial layer 10 is formed on a P substrate 12. A photodiode comprising an N-well collection node 14 with surrounding P-wells 16 is formed in the epitaxial layer 10. The collection node 14 has a conductor 18 attached which carries a signal to a transistor 20, which is part of readout electronics.

The photodiode illustrated in Fig. 1 is a relatively small photodiode, having a width of less than ten micrometers. Typically, such a photodiode will have a width of between four and six micrometers. As also illustrated in Fig. 1, the epitaxial layer 10 has a depth of between four and five μm, and both the N-well and P-wells have a depth of three μm, as measured from the upper surface of the epitaxial layer 10.

Light 22 impinging on the semiconductor produces electron/hole pairs. There is an electron field

around the sense node 14 to attract the electrons there. This electron field is a combination of doping and applied voltage. The position at which electrons e1-e4 are liberated from silicon atoms is a statistical process but is wavelength dependent. For visible light (typical wavelengths from 450nm to 650nm) impinging on silicon, the greatest production of electrons occurs at depths from 1 µm to 5µm. To collect as many electrons as possible, a p-n junction should be provided such that that distance the electrons have to diffuse to the junction is minimised. Thus, a p-n junction at around half this depth is optimal. Therefore, N-Well is usually used to form the p-n junction as it occurs at around this depth.

A problem with this technique is that well implantation is not a critical parameter for CMOS transistors and hence is not particularly well controlled. The width of the collection node 14, shown by X in Fig. 1, varies from part to part and pixel to pixel, by a typical variation dX. The value of dX for the photodiode of Fig. 1 is typically ±300 nm. This variation in the width of the collection node 14 causes variation in the capacitance of the photodiode, leading to the abovementioned problem of mismatch between pixels.

Fig. 2 shows a modification that can be made to the structure of Fig. 1. Here, an N+ implant is used as the collection node. N+ is used to construct a transistor 26, and its implantation is very well

controlled. The part to part and pixel to pixel variation, represented by dX2, in the photodiode of Fig. 2, typically has a value of ±100 nm.

Although this gives a photodiode with a more repeatable capacitance, its shallower depth means that its quantum efficiency is lower. For example, in Fig. 1, photo-generated electrons e1-e3 are most likely to be attracted to the well and be collected. In contrast, in Fig. 2, only e2 will be sensed, with e1 and e3 being lost into the well for the readout circuitry.

Fig. 3 shows a first embodiment of the present invention, which provides a deep yet accurate implant.

Advanced CMOS technologies use a technique called Shallow Trench Isolation (STI) to control accurately the width of (active) N+ or P+ areas. Photo-resist is patterned outside the active areas. Anisotropic etching is used to etch a deep (typically 2μm) trench. This provides a well defined edge for the implants. After implant, polysilicon is deposited inside the trenches.

The present invention provides STI 30 around the collection node 28 in order to provide better control of the width, X, of the collection node 28. As seen in Fig. 3, the N-well collection node 28 and the surrounding P-wells 16 have a depth of 3 μm

below the upper surface of the epitaxial layer 10, and the STI has a depth of 2 μm.

In a method of manufacture of the photodiode, the STI is formed prior to implantation of the N-well, thus providing a definite border for the p-n junction to increase control of collection node 28 width X, with a typical value for dX3 being ±50 nm.

This technique combines the advantage of a deep N-well for better quantum efficiency with better control of implantation and hence capacitance. As dX3 << dX1 we get much better matching than N-Well implant photodiodes.

Ideally, the STI would be as deep, or deeper as the N-Well, as the p-n junction below the STI is a diffuse barrier. However, STI is usually formed at a depth of 2μm, as this is all that is required for transistors. In this situation, two thirds of the diode's capacitance is controlled accurately, which represents an improvement over prior art.

In addition, it is more economical to remain within the standard process flow, rather than producing a new technology which having such an implant.

Fig. 4 illustrates a second embodiment of the present invention, which is applicable for relatively large photodiodes, having widths equal to or greater than ten micrometers. Typically, large photodiodes will have widths between forty and sixty

μm. An N-well collection node 32 is bounded by STI 34. To increase sensitivity, the P-well 16 that is shown in Figs. 1-3 is replaced by P-Epi. This means that all the electrons e1-e4 will most likely be collected by the collection node 32.

The structure of Fig. 4 provides a good solution for photodiodes, but design rule manuals prohibit this implementation for transistor design. Fig. 5 shows a photodiode according to a third embodiment of the present invention. The critical n-p junction is at the N-Well/STI interface and is well controlled. However, the STI 34 of Fig. 4 is extended, so that the STI 38 of Fig. 5 extends over most of the pixel, suppressing P+ and hence avoiding DRC issues.

This structure obtains good matching, but at the expense in a slight (5%) drop in quantum efficiency.

Variations and modifications can be made to the above without departing from the scope of the present invention. In particular, it will be apparent that the conductivity types of the various materials discussed could be reversed, for example, a P-well could be formed in an N-substrate rather than having an N-well formed in a P-substrate.

CLAIMS

1. An image sensing structure comprising a photodiode having a first well of a first conductivity type suitable to act as a collection node, and which is formed in a layer of a second conductivity type, wherein at least an upper portion of the first well is bound on at least part of its horizontally circumscribed perimeter by an insulating trench.

2. The image sensing structure of claim 1, wherein at least an upper portion of the first well is bound on the entirety of its horizontally circumscribed perimeter by an insulating trench.

3. The image sensing structure of claim 1 or claim 2, wherein the trench is a shallow trench isolation (STI).

4. The image sensing structure of any preceding claim, wherein the first well comprises an N-well.

5. The image sensing structure of any preceding claim, wherein the layer of the second conductivity type comprises a P-well.

6. The image sensing structure of any of claims 1-4, wherein the layer comprises a P-epitaxial layer.

7. The image sensing structure of any of claims 1-4, wherein the trench covers a large portion of the upper surface of the photodiode.

8. The image sensing structure of claim 6 or claim 7, wherein an n-p junction is formed at the interface between the trench and the first well.

9. The image sensing structure of any preceding claim, wherein the photodiode has a width of less than ten micrometers.

10. The image sensing structure of any of claims 1-8, wherein the photodiode has a width equal to or less than ten micrometers.

ABSTRACT

(Fig. 3)

A CMOS image sensing structure comprising a photodiode is provided, in which an epitaxial layer (10) is formed on a P substrate (12). The photodiode comprises an N-well collection node (14, 26, 28, 32) formed in an epitaxial layer 10. STI (30, 34, 38) is provided around the collection node (14, 26, 28, 32) in order to provide better control of the width, X, of the collection node (14, 26, 28, 32). The collection node (14, 26, 28, 32) can be surrounded by P-wells (16) or by epitaxial material (10). It can also be surrounded by epitaxial material (10) with the STI (30, 34) being outwardly extended (38) to ensure compliance with existing design rules.

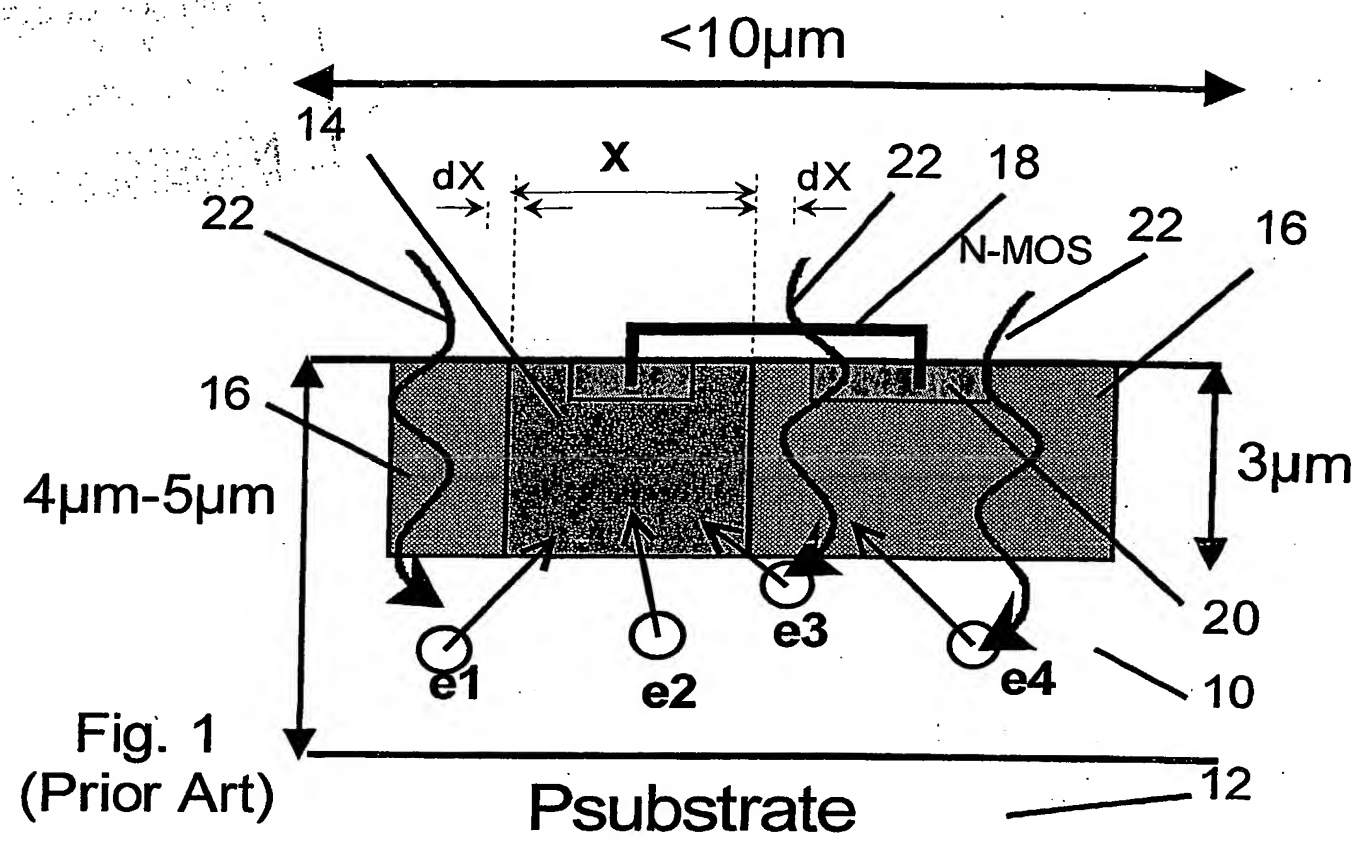

Fig. 1
(Prior Art)

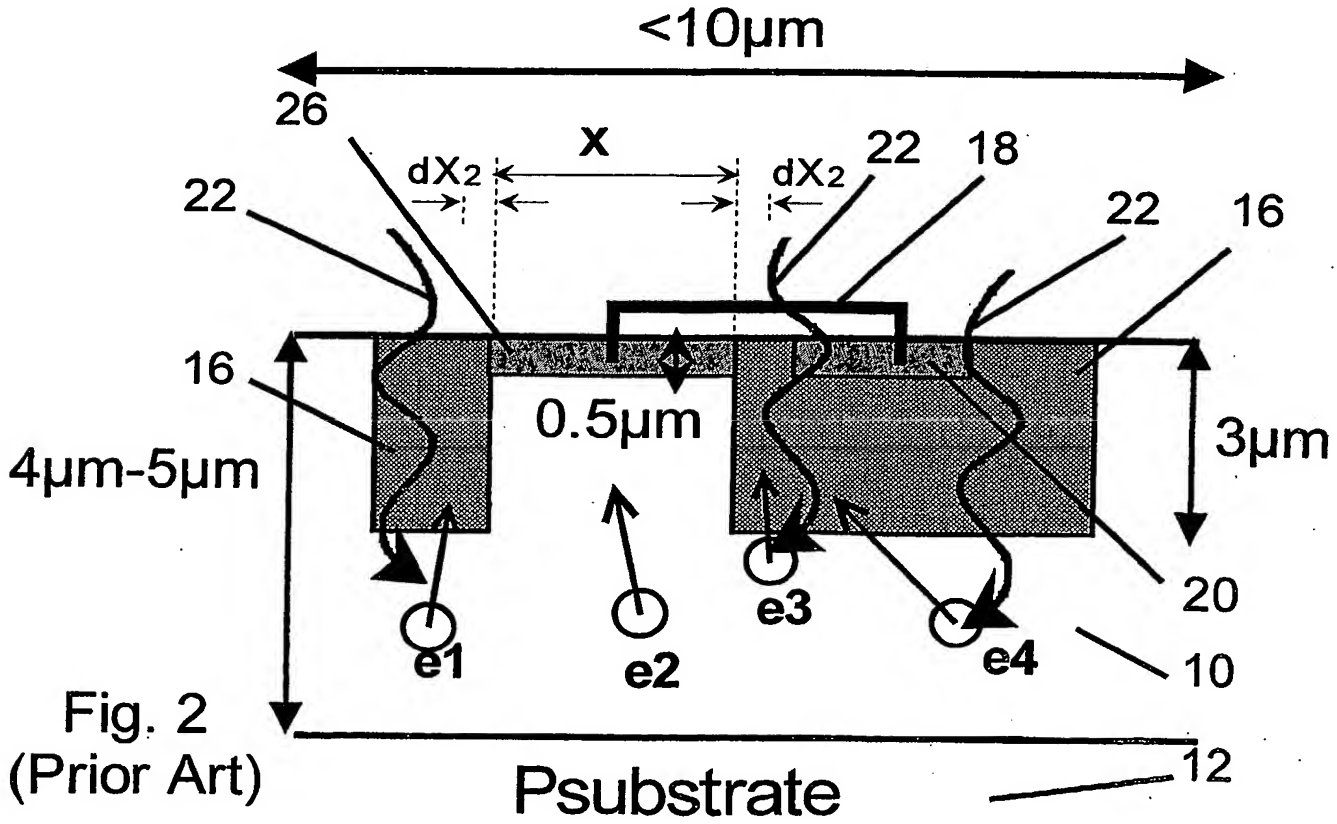

Fig. 2
(Prior Art)

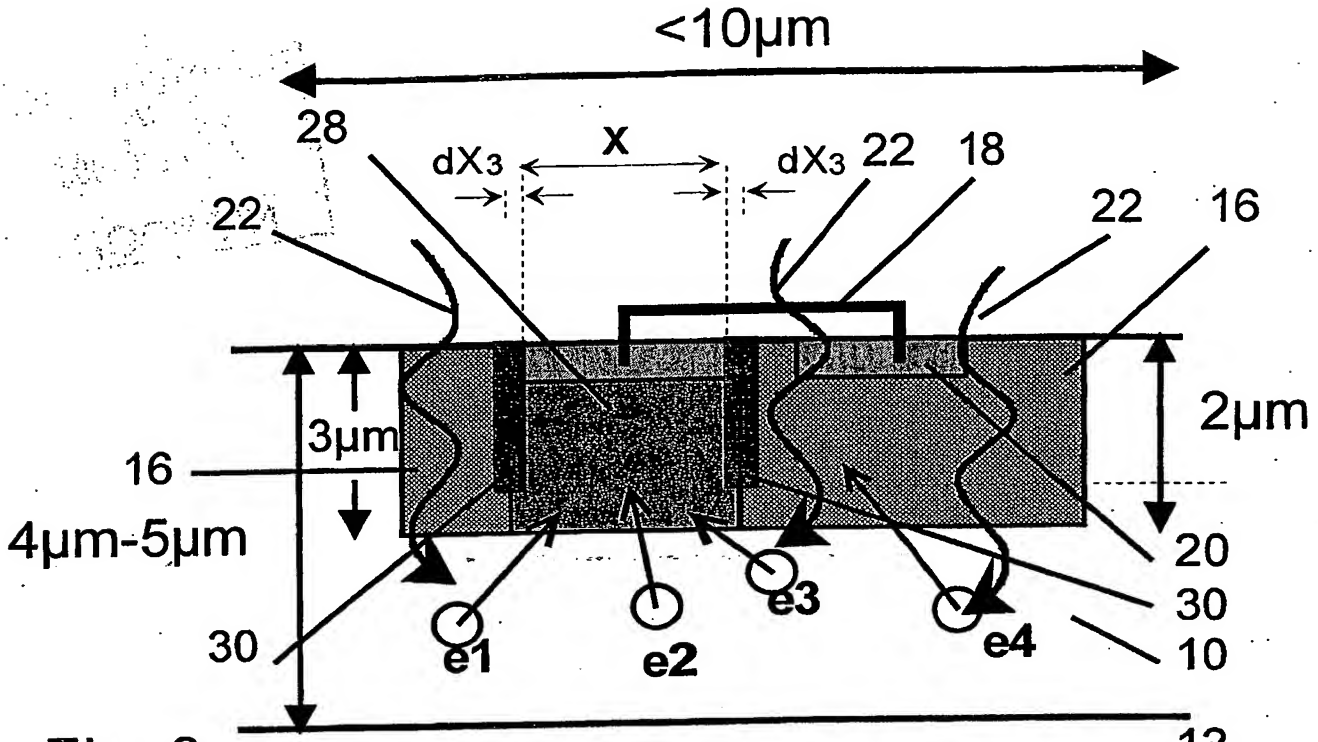

Fig. 3

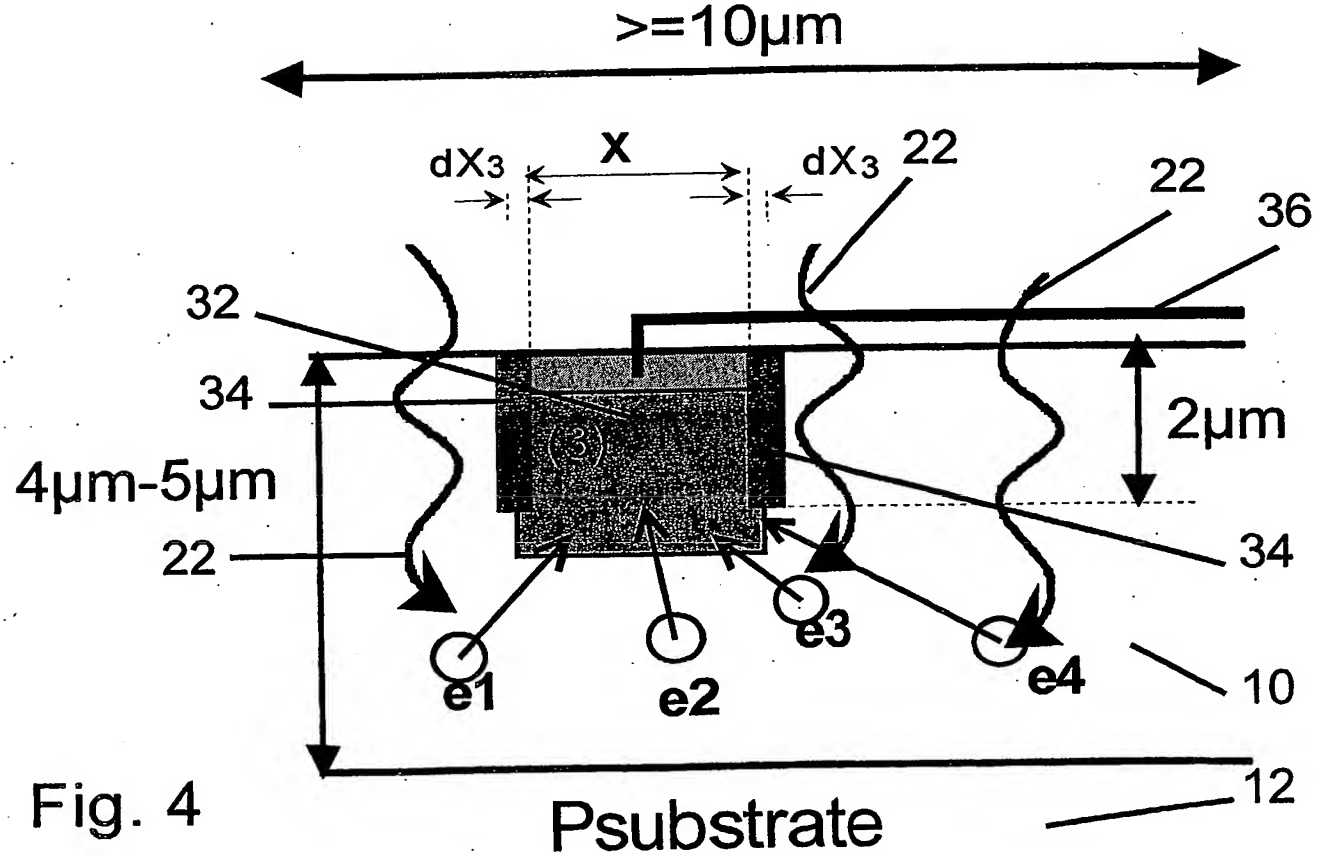

Fig. 4

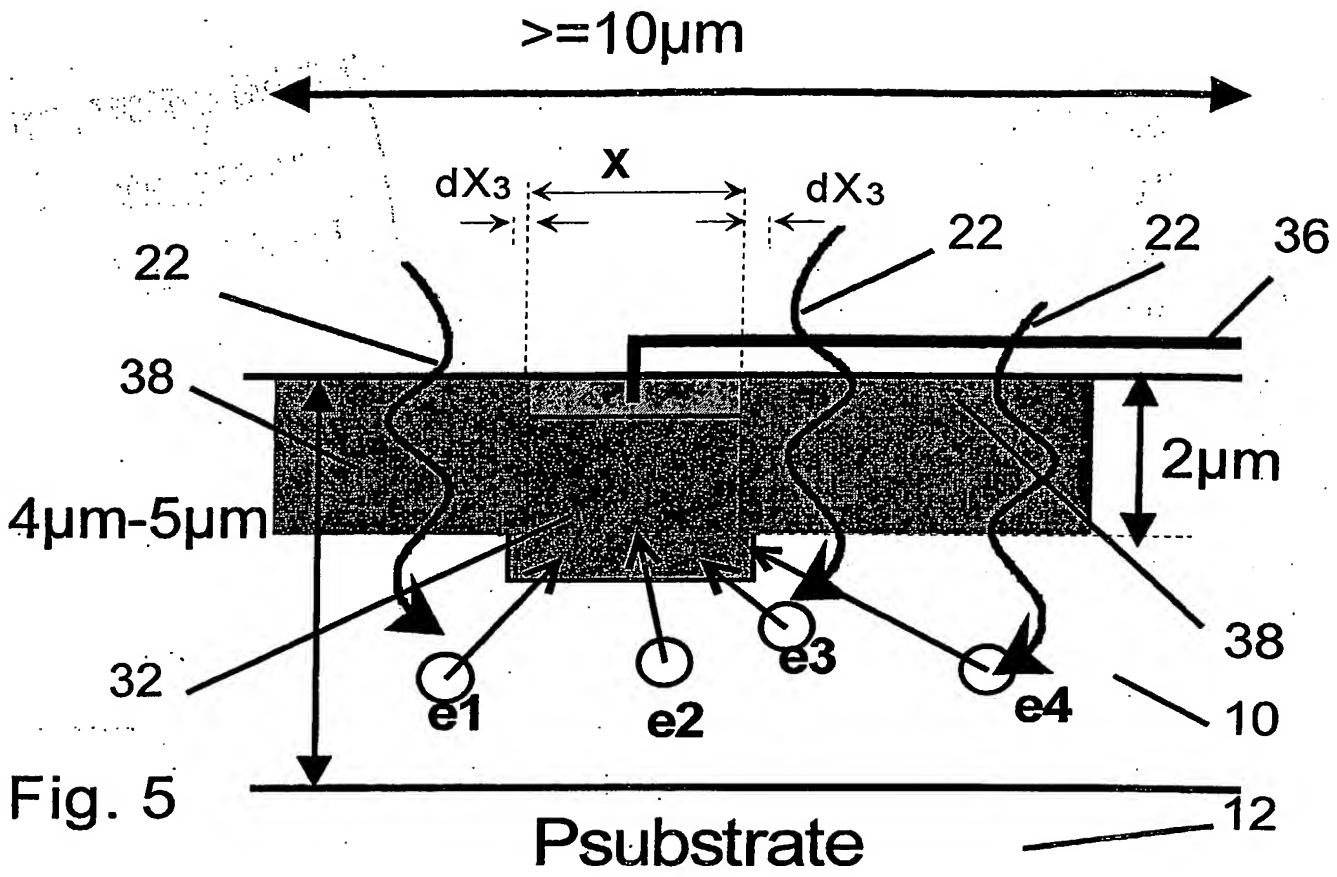

Fig. 5